SKP

Extreme Si Thinning Technologies

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Ultra-thin wafers have various industrial uses such as packaging application (Memory ,TSV, interposers, WLP, LEDs, power device, CMOS Image sensor, MEMS RF Devices, and RF device.

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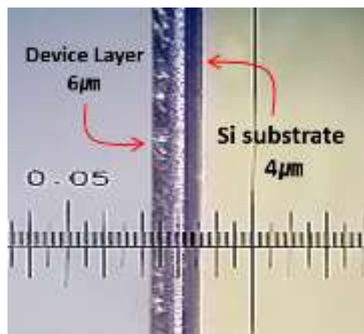
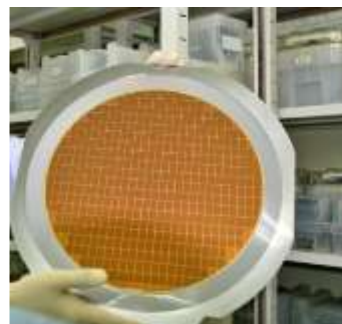
02

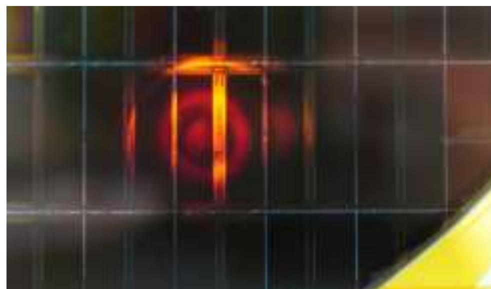
Examples of extreme-wafer thinning implementation by chemical polishing

THK : 10 ㎛t NAND flash memory wafer

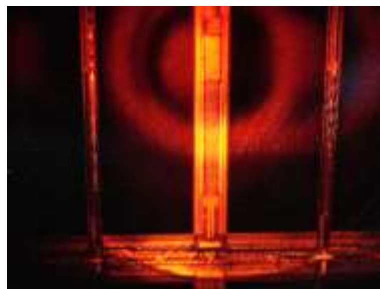




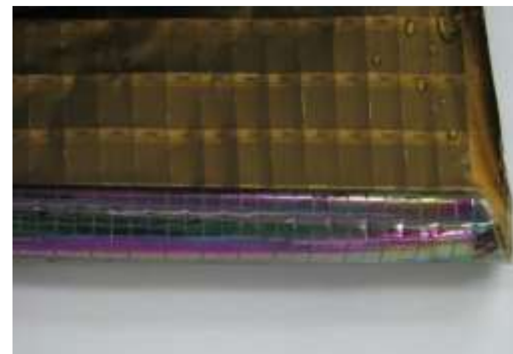
12inch 50 µmt Memory wafer thinned down to 15 µmt



NAND flash memory Transmission of 6 ㎛t

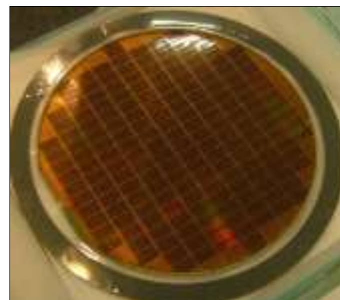


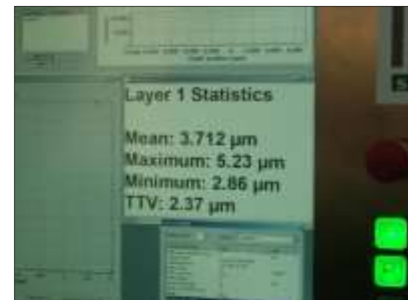
Enlarged image



Bulk Silicon is completely removed, leaving only the device layer

Non-contact measuring by ISIS





Thickness measurement result after thinned down 200 ㎛t to 3 ㎛t

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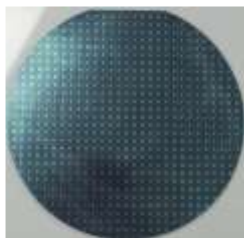
Implementation of extreme thinning chip by new etchant



50 µmt wafer ground by DBG

Back side

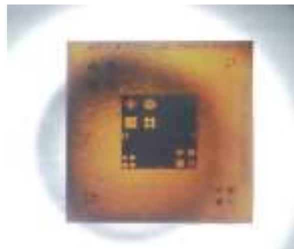
5*5mm, 50 µmt chips

50 µmt chip on protecting tape for thinning

Dip etching

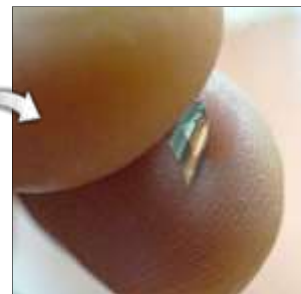
thickness 50 µmt Vs 6µmt

Measurement
6µmt



thickness : 6 µmt transmission

Before thinning: 50µmt



After thinning:6 µmt

Bendable chip : 5*5mm , 6µmt

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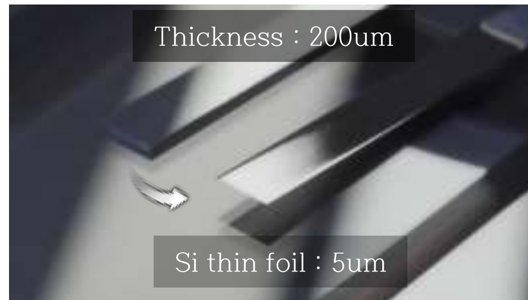
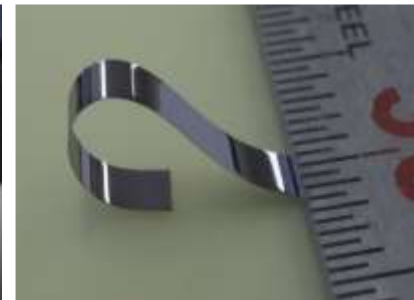
04 Physical properties of extremely thinned silicone materials

Bendable memory chip
Thickness : 25 ㎛t

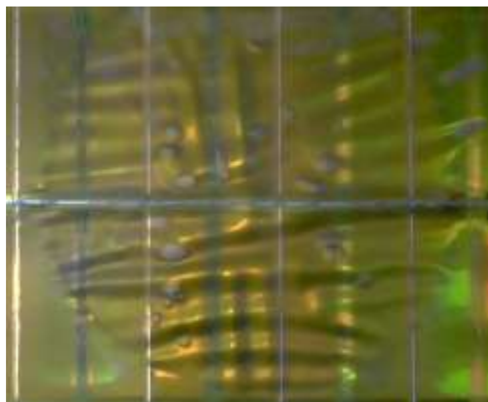
Extreme thinned chip
Thickness : 8 ㎛t



Extreme thinned bare Si : 5 ㎛t

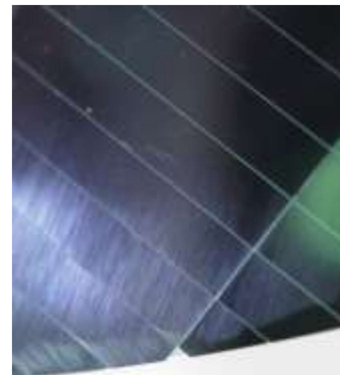


Bendable Si : 5 ㎛t



▲ front side

▲ Back side



Ground Si : 200 ㎛t

Bendable Si : 10 ㎛t

Active layer covered with cellulose tape
Heat shrinks, but thin Si-wafer (10 ㎛t)does not break

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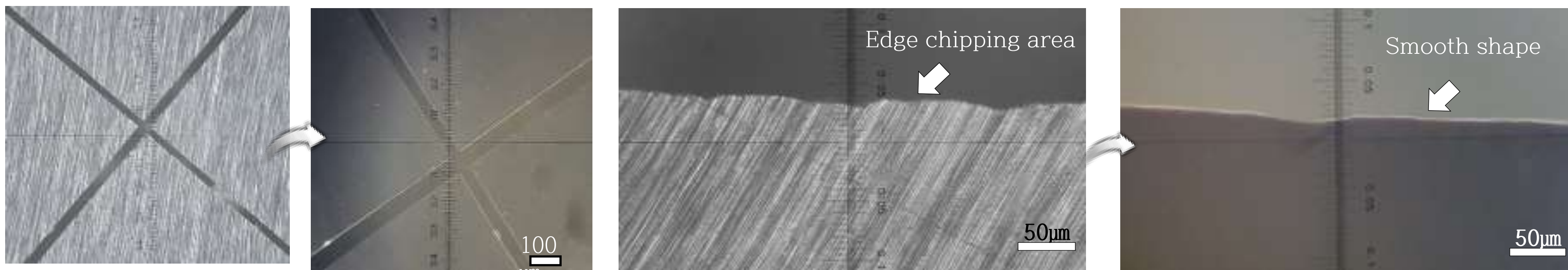
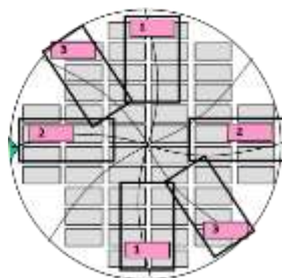
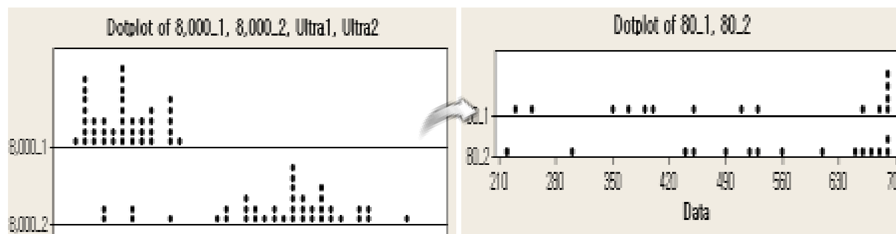
Effects of chemical polishing (SSD relief & thinning)



Fine ground roughness Vs after chemical polished surface , change to smooth , mirror surface and wheel mark removed



#12,000 grit ground 12 inch DBG Wafer
use of #4800 dicing saw



Die strength becomes uniform after chemical etching.

✓ Flexibility of Ultra thinned patterned wafer

Grinded wafer : 2,000grit ,
THK: 200 ㎛t

Mirror surface: damage relief
and thinning

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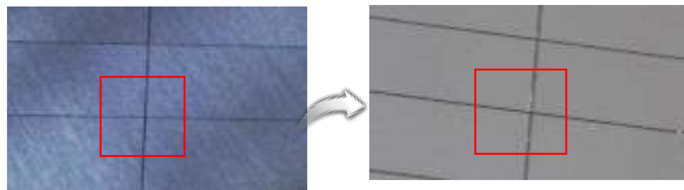
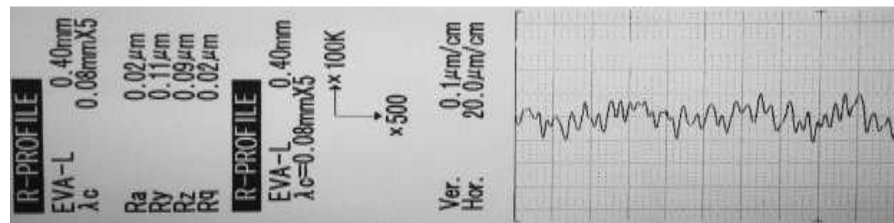
06 Removal of damage layer and improvement of surface condition by chemical polishing

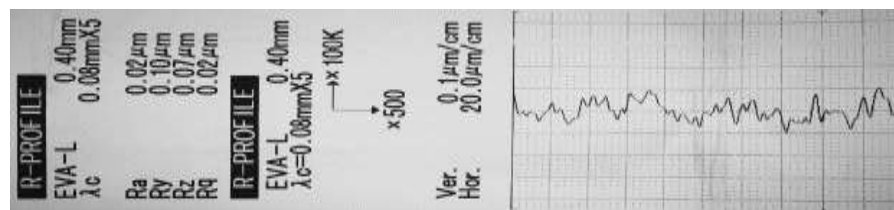


DBG #2,000 grit
surface ground

After Damage
Relief surface

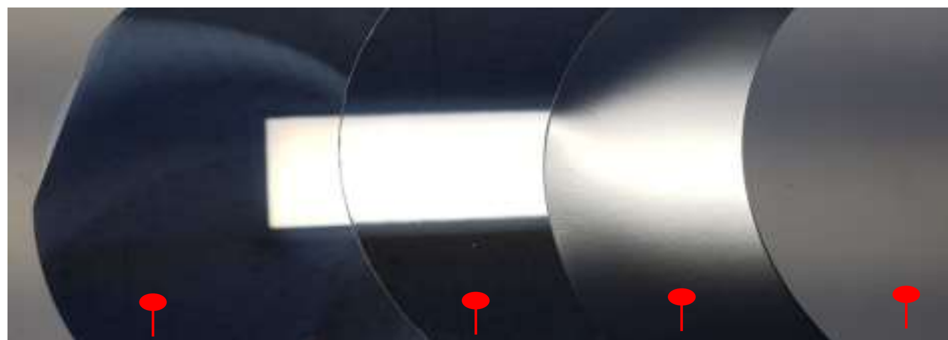


Ra : 0.02
Ry : 0.11



Ra : 0.02
Ry : 0.10

Ground roughness Vs after thinning roughness



#2,000 fine ground	Mirror like C.P	IR-4031 C.P	Texture etching
Ra : 0.02 Ry : 0.11	Ra : 0.02 Ry : 0.10	Ra : 0.11 Rt : 0.96	Ra : 0.33 Rt : 2.43

Textured
surface image

We have been developing and will promote the diversification of the etched surface according to the needs of users.

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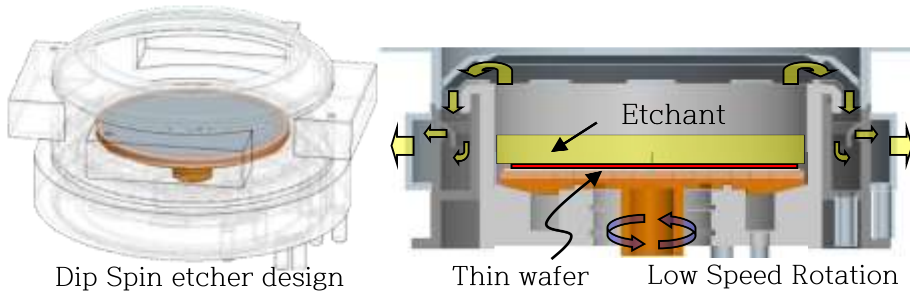
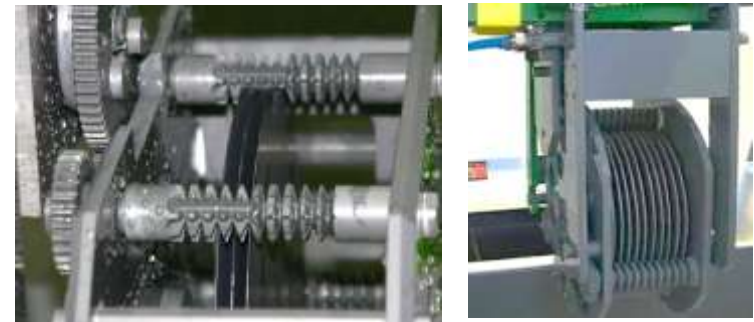
Design of the Dip chemical Polishing equipment(Single wafer processing , barrel and dip type)



Dip Spin etcher design



Barrel etcher for ultra thinning or damage relief

Dip-Spin thinning

Ground DBG wafer — Dip etching — Thinned wafer

Ground wafer — Thinned wafer

Method 1 : Dip Spin type method (single wafer processing)

→Continuous production is possible with single wafer processing.

Method 2 : Barrel type method (batch type)

→ It is possible to thinning several wafers at once.

Method 3 : Dip method (equip' design required)

→ Thinning by attaching to a protective tape

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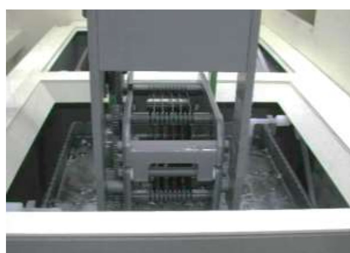
- Develop of wafer thinning equipment

8inch proto(dip-spin) Thinning chamber
Thinner(made in 2008)

12inch proto
Thinner(made in 2008)

Thinning chamber

8inch proto(Barrel)
Thinner(made in 2006)



Thinning chamber

We have produced various thinning equipment in the past,
and recently, we are developing the most suitable equipment.
In particular, the main point of Etchant's improvement is that the surface roughness is improved(mirror-like) and no harmful gas (NOx) is generated during etching.

8inch wafer mass production equipment : 150um→50um ,
16wph (made in 2007)

Thinning chambers

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- Wafer thinning method using carrier tool (wafer and ring flame)

Barrel etcher (prototype)

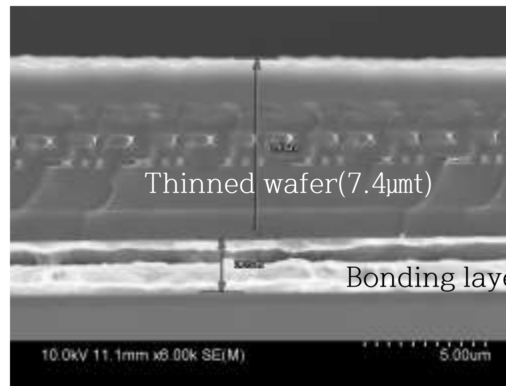
wafer on ring frame

ring frame on barrel module

wafer on ring frame

Wafer supported by ring frame is inserted into rotating barrel

Support wafer(bottom)



Barrel with wafers

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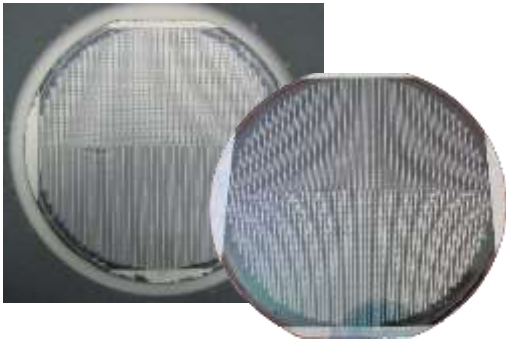
Thin-film device manufacturing by new etchant

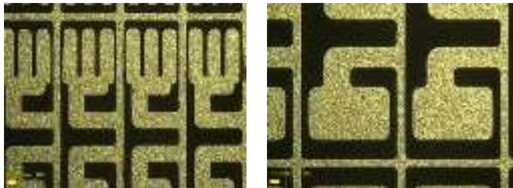
SKP

→ Damage free ultra-thin flexible device film enables pick-up and transfer

This work presents a novel method entitled “device transfer by backside etching (DTBE)” for transferring thin-film devices from Si wafers to a glass or plastic substrate. First, high performance poly-Si thin-film transistors (TFTs) were fabricated on a Si wafer and then adhered to UV tape substrates. The remaining Si was removed delicately using wafer backside grinding and wet chemical etching.

■ thin-film device (Micro-Sensor) Manufacturing Technology





UV tape

Silicon micro sensor

Enlarged Image

Line width : 20~40um / thickness 20um , method : dip etching

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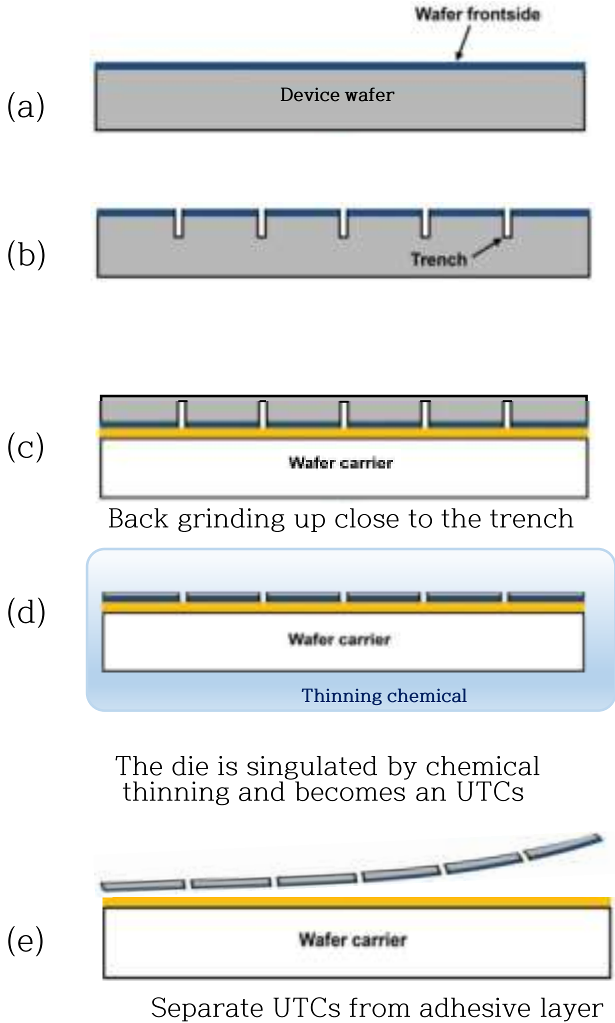
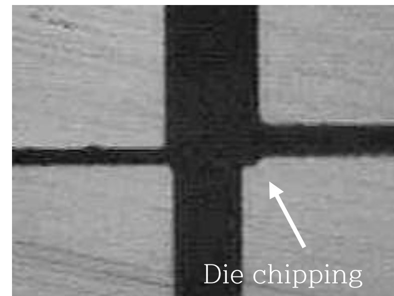
New extreme thin chip processing by new concept

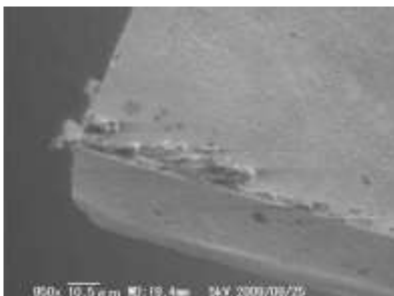


△ Schematic of Super thinning By back grinding + wet etching

Problems of Existing DBG Grinding

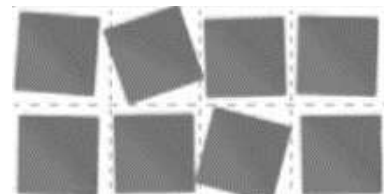


△ distorted die

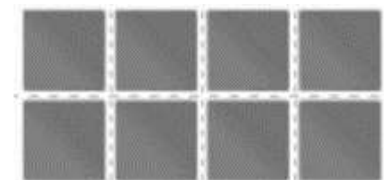


△ dust remains

1) Chipping of die edge
2) Dust remain in the die space
3) Die spacing is distorted

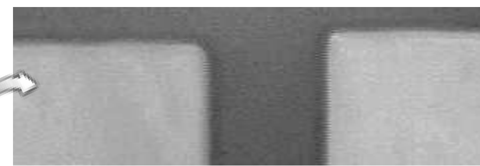


→ Distorted chip after grinding



→ NO distorted chip after New chemical etching method

✓ Die chipping



✓ Smooth of die edge

Electronic chips of 10 ㎛ or less can be processed through a wafer chemical polishing process (grinding and wet etching) using a carrier wafer.

In order to obtain an ultra-thin chip, the depth of the trench can be minimized to reduce processing time and side damage, and a chip with a good quality edge can be obtained.

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Comparison of ultra-thinning methods

Extreme thinning	ADP-DCE (Plasma)	CMP	Chemical polishing (New Method)
Purpose of the process	damage relief	damage relief	Extreme thinning
Cost of process contributes	**high capital cost** Plasma processes usually require expensive equipment and etching gases	**high material cost** Processes use expensive slurries and critical post-cleaning steps	**Low capital & material cost**
Defects after thinning	amorphous layer about 0.2 um thick and electrically active defects are created. needle-like hillocks created	high pressure (300~500 gf/cm^2) exerted by the CMP process remains potential defect	Stealth defects are removed Leave only the denuded zone
Removal-Rate[μm/min]	10~20	0.5~1	10~20
Uniformity between wafer(8~12")	< 2% after removing 20 μm	10% after removing 20 μm Uneven wafer thickness, at the wafer edge.	<1% after removing 50 μm
Possible removal thickness [μm]	>10um (Impassible uniformity over 10μm off)	>10um (Impassible uniformity over 10μm off)	>100 um (Uniformity is maintained even with 100μm thinning)
Die strength	High(10μm off max.)	Middle(5μm off max.)	Very high(>25μm min.)

Wet chemical Etching method	Spin etcher (Current Method)	Chemical polishing (New Method)
Process parameter	Chemical spin etch	Chemical dipping or barrel etch
Composition & feature of chemicals	$HF+HNO_3+DI$ + α (H_2SO_4 / H_3PO_4) very dangerous, Fuming chemical	Fluoride + Oxidizer + α + β Do not contains HF & HNO_3 Relatively stable formula, No fuming chemical
Reaction gas generation	NOx gas generation	NOx gas free
Etch-Rate [μm/min]	2~20	2~20
TTV between wafer (8~12")	Less than 2.5 (10μm off max.)	Less than 2.5μm (<150μm off) Less than 1.0μm (<50μm off)
Possible removal thickness [μm]	>10um (Impassible uniformity over 10μm off)	>100 um(Uniformity is maintained even with 100μm etching)
Die strength	High (10μm off max)	Very high (<50μm off)

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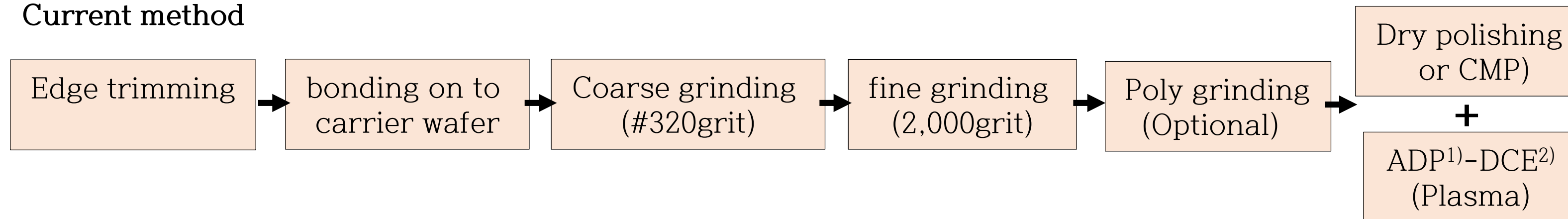
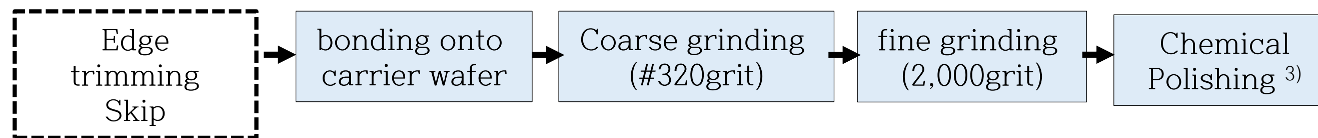
Method of Extreme thin wafer (Current Vs New method)





1)ADP : Atmospheric Downstream Plasma)
2)DCE : Dry Chemical Etching)
3)Chemical Polishing : Use of new etchant

<Recommendation of Si Ultra thinning flow 3 step>

→ Bonding onto carrier wafer → Coarse grinding & fine grinding (thin down to 50㎛ ~30 ㎛)

→ Chemical polishing (thin down to 20 ㎛~5 ㎛)

Wafer back grinding equipment manufacturer in Japan

DISCO (DBG8761): Coarse grinding(#320grit) → Fine grinding(#2,000grit) →Poly grinding or dry polishing(2㎛ removal) → CMP (optional)
ACCRETECH : PG3000RMS: Polish grinder) OKAMOTO : (GDM300:Backgrinder & Polisher)

Single wafer spin etching equipment companies in the world
Ram research , Veeco(SSEC)

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Review and Promotion Direction

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<summary>

1. Extreme thinning of wafer and chip
2. Removing of sub surface damage after grinding
3. Equipment Concept Development
 1) Dip-spin concept (single wafer processing)
 2) Barrel dip concept (batch type processing)
 ** wafer support : carrier wafer or protecting tape and frame
4. Evaluation items for applying new technology

▷ etch rate according to formulation ▷ uniformity (TTV) ▷ surface roughness ▷ die strength ▷ reproducibility
▷ throughput ▷ noxious fume free ▷ metal contamination ▷ penetration to adhesive layer ▷ raw material cost
▷ foot print of equipment ▷ equipment cost ▷ operational cost ▷ variety of method ▷ chemical reusability and recycling

<Target>

Through the formulation of a new concept of silicon etchant, it replaces existing applied technology and commercializes a new applied method to provide necessary technology and build a business partner, and supply self-developed original technology to domestic and overseas markets.

<Load map for evaluating the applicability of etchants and equipment to the industry (draft)>

1) Obtaining specimens(wafer) for testing
2) Preparation of the tools for testing (lab level) and test specimens for the evaluation
3) Promotion of joint development in connection with related research institutes and related companies
4) Promote application of technology to domestic and foreign companies after completion of technology evaluation and verification

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